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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,295	06/24/2003	Yoshiyuki Arai	10873.1243US01	9034

23552 7590 02/21/2006

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,295	ARAI ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *13-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5-8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen et al. (US 6707140), hereinafter Nguyen.

Regarding claim 1, Fig. 7 of Nguyen shows a semiconductor device comprising:

a substrate [120, 130];

a plurality of semiconductor chips [110, 155] mounted on the substrate by stacking one on top of another; and

an encapsulation resin layer [135; col. 4, lines 22-23],

wherein, among the plurality of semiconductor chips, a first semiconductor chip [155] as an uppermost semiconductor chip is mounted with a surface thereof on which a circuit is formed facing the substrate, wherein the first semiconductor chip is directly and electrically connected to bumps [115, 150] and a second semiconductor chip [110] provided immediately below the first semiconductor chip is directly and electrically connected to the bumps (col. 4, lines 52-59) wherein the encapsulation resin layer is formed so that at least a surface of the first semiconductor chip opposite to the surface on which the circuit is formed and a part of side

surfaces of the first semiconductor chip are exposed to the outside of the encapsulation resin layer.

Regarding claim 3, Fig. 7 of Nguyen shows that the bumps are from solder [solder bumps; col. 4, lines 54-56].

Regarding claim 5, Fig. 7 of Nguyen shows that among the plurality of semiconductor chips, a lowermost semiconductor chip is electrically connected to the substrate via a wire [125].

Regarding claim 6, Fig. 7 of Nguyen shows that the bumps form a space between the first semiconductor chip and the second semiconductor chip, and the space is filled with the encapsulation resin of the encapsulation resin layer.

Regarding claim 7, Fig. 7 of Nguyen shows that the substrate is a lead frame.

Regarding claim 8, Fig. 7 of Nguyen shows that among the plurality of semiconductor chips, a lowermost semiconductor chip is bonded to one surface of a die pad portion [120] of the lead frame, and wherein the encapsulation resin layer is formed so the other surface of the die pad portion is exposed to the outside of the encapsulation resin layer.

Regarding claim 1, Fig. 8 of Nguyen shows a semiconductor device comprising:

a substrate [120, 130];

a plurality of semiconductor chips [110, 155] mounted on the substrate by stacking one on top of another; and

an encapsulation resin layer [135; col. 4, lines 22-23],

wherein, among the plurality of semiconductor chips, a first semiconductor chip [155]

as an uppermost semiconductor chip is mounted with a surface thereof on which a circuit is formed facing the substrate, wherein the first semiconductor chip is directly and electrically connected to bumps [115, 150] and a second semiconductor chip [110] provided immediately below the first semiconductor chip is directly and electrically connected to the bumps (col. 4, lines 52-59) wherein the encapsulation resin layer is formed so that at least a surface of the first semiconductor chip opposite to the surface on which the circuit is formed and a part of side surfaces of the first semiconductor chip are exposed to the outside of the encapsulation resin layer.

Regarding claim 11, Fig. 8 of Nguyen shows that a heat dissipater [123] is provided on the surface of the first semiconductor chip exposed to the outside of the encapsulation resin layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen in view of Hikita et al. (US 6133637), hereinafter Hikita.

Regarding claim 2, Fig. 7 of Nguyen shows most aspect of the instant invention except

"among the plurality of semiconductor chips, a lowermost semiconductor chip is bonded to the substrate with an adhesive." Fig. 33 of Hikita shows a multi-chip package wherein among the plurality of semiconductor chips, a lowermost semiconductor chip [14] is bonded to the substrate [12a] with an adhesive (col. 15, lines 47-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hikita into the device of Nguyen in order to have the lowermost semiconductor chip bonded to the substrate with an adhesive to secure device to the substrate.

Regarding claim 4, Fig. 7 of Nguyen shows most aspect of the instant invention except "a portion of the first semiconductor chip is bonded to a portion of the second semiconductor chip with an adhesive." Fig. 33 of Hikita shows a multi-chip package wherein a portion of the first semiconductor chip [16] is bonded to a portion of the second semiconductor chip [14] with an adhesive (col. 15, lines 54-58).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hikita into the device of Nguyen in order to have a portion of the first semiconductor chip bonded to a portion of the second semiconductor chip with an adhesive to strengthen the bond between two chips.

Regarding claim 12, Fig. 8 of Nguyen shows most aspect of the instant invention except "the heat dissipator is a metal film or a metal heat sink." Fig. 33 of Hikita shows a multi-chip package wherein the heat dissipater [30] is a metal heat sink (col. 16, line 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention

was made to incorporate the teachings of Hikita into the device of Nguyen in order to have the heat dissipater to be a metal heat sink to transfer the heat efficiently.

Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen in view of Pu et al. (US 6610560), hereinafter Pu.

Regarding claim 9, Fig. 7 of Nguyen shows most aspect of the instant invention except "on a second semiconductor chip provided immediately below the first semiconductor chip, a third semiconductor chip is mounted along with the first semiconductor chip." Fig. 2D of Pu show a second semiconductor chip [210] provided immediately below the first semiconductor chip [220], a third semiconductor chip [230] is mounted along with the first semiconductor chip.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Pu into the device of Nguyen in order to have a second semiconductor chip provided immediately below the first semiconductor chip, a third semiconductor chip mounted along with the first semiconductor chip to have a compact package.

Regarding claim 10, Fig. 2D of Pu shows that both the first semiconductor chip and the third semiconductor chip are electrically connected to the second semiconductor chip via bumps.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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